IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the present application:

1-43. (Canceled)

44. (Currently amended) A processor comprising:

~~a plurality of~~at least three functional units coupled to each other to execute operations defined from an instruction set of the processor, the ~~plurality of~~at least three functional units including an arithmetic logic unit (ALU) and a multiplier, the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including

a RISC/CISC assembly code level,

a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units, and

a vector processing assembly code level, using which an individual instruction can be used to cause an operation to be automatically repeated sequentially a programmable number of times on different data words; ~~and~~

a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis; and

a bus routing structure that includes at least three dedicated output buses, including a separate dedicated output bus for each of the at least three functional units, each of the at least three dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses.

45. (Previously presented) A processor as recited in claim 44, wherein the second assembly code level comprises a native machine language of the processor.

46-48. (Canceled)

49. (Currently amended) A processor as recited in claim 44, further comprising:

~~a plurality of dedicated output buses, one for each of the functional units; and~~

~~a plurality of~~at least three bus registers, each coupled to store the output of only a corresponding one of the ~~plurality of~~ at least three functional units and each coupled to only a corresponding one of the ~~plurality of~~at least three dedicated output buses.

50-62. (Canceled)

63. (Currently amended) A processor comprising:

~~a plurality of~~at least three functional units coupled to each other to execute operations defined from an instruction set of the processor, the ~~plurality of~~at least three functional units including an arithmetic logic unit (ALU) and a multiplier, the instruction

set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including

a RISC/CISC assembly code level,

a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units, wherein the second assembly code level comprises a native machine language of the processor, and

a vector processing assembly code level, using which an individual instruction can be used to cause an operation to be automatically repeated sequentially a programmable number of times on different data words;

a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the special use control registers, by which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis;

~~a plurality of~~at least three dedicated output buses, one for each of the at least three functional units, each of the dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, wherein each of the dedicated output buses is coupled to an input of at least one other of the plurality of functional units, and each of the functional units has an input coupled directly to one of the dedicated output buses; and

a plurality of bus registers, each coupled to store the output of only a corresponding one of the plurality of functional units and each coupled to only a corresponding one of the plurality of dedicated output buses.